



Technology Drives New Stencil Applications

With new stencil designs, printing can occur for small and bulky components on the same PCB, wafer-level and flip-chip package mounting, and 3D packaging interconnections, among other applications. 3D electroformed stencils might be the next step for stacked die inside packages, printing solder for die-to-die interconnects.

Although the stencil is commonly recognized as a simple tool used in the printing process, its uses are continually evolving. Normally, it is used to print solder paste on pads of the PCB as the first step in surface mount assembly. After the paste bricks are printed, components are placed in solder paste while it is still tacky. Next, the PCB is heated in a reflow oven to melt the paste and form a solder joint at each component lead.

As with the entire manufacturing sector in today's challenging economy, the electronics industry has ongoing initiatives to improve productivity, cut costs, and reduce package sizes. This constant push to increase speed and reduce component size has made the printing function more complex.

Smaller component packages require higher-density I/O leads and, therefore, smaller pads on the PCB. Small pads require small stencil apertures. The resulting increased focus on stencil technology has led to greater breadth in its applications.

Stencil printing is a two-phase process. First, the solder paste is forced into the stencil aperture as a squeegee blade wipes over the surface (fill stage). Second, solder paste pulls out of the stencil aperture onto the PCB pads when the PCB separates from the stencil (transfer stage). The

transfer stage can be conceived of as a tug of war: the aperture walls are trying to hold back the solder paste and the pad on the board is trying to pull the paste out of the aperture. The ratio of the inside aperture wall area to the area of the pad beneath the aperture opening determines who will win the tug of war.

The smaller the aperture, the thinner the stencil needs to be to achieve an area ratio that promotes good paste transfer. This is a problem when very small component packages like 300- μm -pitch CSPs and 01005 chip components coexist on a PCB with RF shields and *SMT* connectors. The smaller components require a thin stencil for good paste transfer and the larger components need a thick stencil to achieve the needed paste height to resolve any coplanarity issues.

Step stencils are a possible solution, however, there are limitations dictated by the spacing between apertures in the two stencil thicknesses. If these apertures get too crowded, there is insufficient space to allow good paste fill for apertures in the thinner stencil portion. It is not unusual to find this occurring in the manufacture of cell phones and other handheld devices where small apertures are close to the RF shields.

Another solution is the two-print stencil system. In this case, a stencil is used to print the small component apertures with a stencil thickness optimized for good paste transfer. A second stencil is used to print the larger apertures (RF shield and *SMT* connectors) where more paste height is required. This second stencil has relief pockets formed on the PCB side of the stencil anywhere paste was printed with the first stencil. After printing with both stencils, the PCB goes to pick-and-place then on to reflow.

Design guidelines for the two-print stencil system stencil will be presented at the IPC APEX Expo 2009 in Las Vegas.¹

Stencils are useful beyond printing solder paste. Thin electroform stencils (around 35- μm thick) can print flux on substrates prior to flip-chip die placement. The two-print system also is useful for flip-chip assembly where the second stencil prints solder paste for chip components while having a relief pocket for the flux printed by the first stencil in the system.

More stencil applications are appearing in the wafer-level packaging (WLP) arena. Electroform stencils print solder paste onto wafer die pads. An electroform stencil, 50- μm thick with 150- μm apertures, prints solder bricks on each die pad (~500,000 apertures), which form solder bumps once the wafer is reflowed.

Electroform stencils are also used in ball drop applications at the wafer level. The first step in this process is to print flux on each pad on the wafer. Typically, this stencil is in the range of 35- μm thick. Next, a ball drop stencil, with apertures typically equal to ball size + 75 μm , is used as a tool in the ball drop process. In some cases, stand-offs are built up on the bottom side of the ball drop stencil to keep it from touching the printed flux.

Interesting research is being performed in the area of stacked die packages using 3D electroform stencils to print connections from die to die in the die stack. Perhaps this will become the next application for the ever-evolving stencil. **SMT**

REFERENCES:

1. "Stencil Design When 01005 and .3mm Pitch μ GBA Coexist with RF Shields," William E. Coleman, S24 Paste and Printing II, APEX 2009, Wednesday, April 1, 1:30 pm–3:30 pm.

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